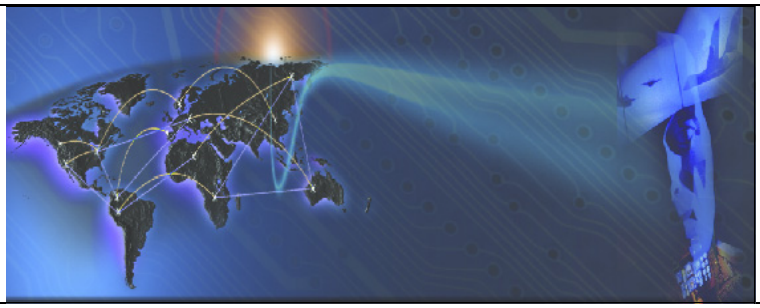


PCI-RMS HARDWARE

FEATURES

- DMA Engines
- Error Detection and Recovery
- 1.0625 Gigabits Per Second Fiber Channel
- Onboard/Offboard Memory with Spinlock Support
- PC, Workstation, Server, and Enterprise Class System Use

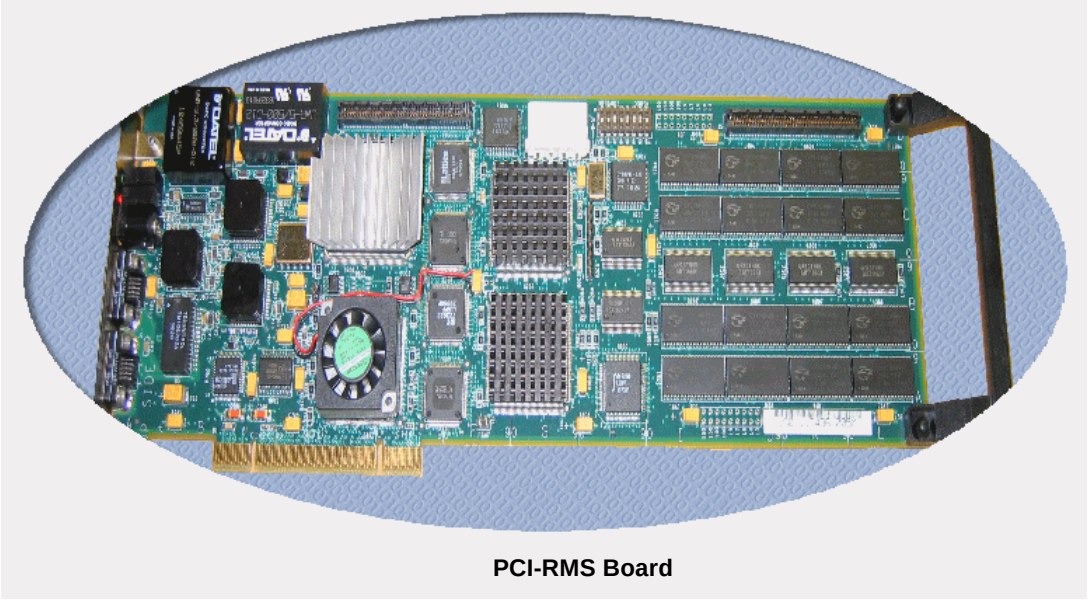
BENEFITS

- Affordable and Easy to Install
- Simple Programming Model
- High Performance Real-Time Clusters
- Windows XP®, NT4®, Linux®, Solaris®, and HP® Tru64 Compatible

PCI-based Reflective Memory (PCI-RMS) is a high performance multiprocessor distributed memory system that sets a new standard in the Reflective Memory family of technologies. It is the latest innovation from COMPRO in high-speed deterministic system connectivity and continues in the tradition of Reflective Memory and Memory Channel interconnects.

PCI-RMS is the basis for creating an industrial strength Real-Time cluster with hundreds of nodes in a single ring. The cluster can be configured using many different microprocessor families, motherboards, and operating systems to form a truly open heterogeneous environment.

PCI-RMS is an affordable solution to your data distribution needs. COMPRO supplies the product with a shielded twisted-pair copper cable media of the highest quality. The PCI-RMS design enables you to pick a platform to fit your project needs with quality, performance, and affordable choices. It is what you expect from the company that invented Reflective Memory.



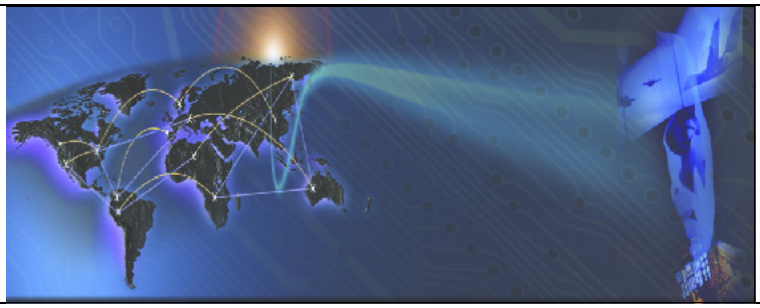
PCI-RMS Board

Fiber Channel Connection

High performance and low latency are the hallmark of PCI-RMS. Using COMPRO's master/master ring topology, up to 254 point-to-point flow controlled segments can be configured to form a ring up to 7.8 km long (100 feet between nodes, up to 254 nodes).

The advantage of using this modified Fiber Channel-2 layer approach is it enables a simultaneous transfer of data from every node to traverse the entire ring (multipoint-to-multipoint). Imagine, 254 nodes able to broadcast and receive at a given instance in time without tokens or data collisions in less then 300 microseconds.

The Fiber Channel shielded twisted-pair cable provides the highest data transfer capability of up to 1 Gigabit per second with the lowest cost per connection.



Memory Features

PCI-RMS memory operation and options are extremely flexible so you can make use of the onboard spinlock, PCI, and DMA memory features simultaneously.

The circuit board is configured with 8 MB of physical SRAM memory. Up to 256 MB of system memory on the node CPU can be addressed and used in conjunction with the circuit board SRAM memory.

The onboard SRAM can be used as hardware-assisted Spinlock Reflective Memory, providing registered return receipt data transfers for added message delivery assurance.

PCI-RMS features low data latency of less than 5 microseconds, broken out as follows:

- 2 µsec for PCI memory to link
- 1 µsec per node
- 2 µsec for link to PCI memory

The Reflective Memory design has two DMA engines with which you can configure the logic circuit to function in Memory Channel mode and relieve the CPU of cycle-stealing tasks such as moving blocks of memory-resident data. The two onboard DMA engines can move blocks of data at industry-leading speeds with less than 20 µsec start-up latency.

If forwarding across multiple nodes is required, an average only of 1 µsec latency per node is incurred. This permits data to be written to all the nodes on the link before it is written to the source node's memory.

In this manner, you can broadcast data sets to nodes in the cluster (point-to-multipoint) and create a deterministic I/O mechanism.

Error Detection and Recovery

In addition to the high performance and flexibility of the PCI-RMS, COMPRO has included features to assure your Real-Time cluster is manageable and your data is reliable. The PCI-RMS has an extensive set of error detection and software recovery techniques for enhanced data integrity.

These techniques include: Cyclic Redundancy Checks (CRC) on Serial Data Frames, Bus and Parity Error Reporting, visual status indicators, and software-accessible status registers.

Serial Link Error Handling

For reliability of data communication between connected Reflective Memory nodes, a hardware interrupt can be generated to report Serial Link errors when the serial link fails or a data transfer error is encountered.

DMA Complete and Mailbox Interrupts

Mailbox interrupts are used to asynchronously notify a node upon the arrival of data at the node. Nodes also can be asynchronously notified by a DMA Complete interrupt upon the completion of a local DMA transfer.

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